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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,357	02/06/2002	Michael D. Kilgore	M-11543 US	4288
34036	7590	02/28/2006	EXAMINER	
SILICON VALLEY PATENT GROUP LLP			GUERRERO, MARIA F	
2350 MISSION COLLEGE BOULEVARD				
SUITE 360			ART UNIT	PAPER NUMBER
SANTA CLARA, CA 95054			2822	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/072,357	KILGORE, MICHAEL D.	
	Examiner Maria Guerrero	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 14 December 2005.
- 2a) This action is **FINAL**.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-16, 18 and 25-28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-4, 6-16, 18 and 25-27 is/are rejected.
- 7) Claim(s) 5 and 28 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                     | Paper No(s)/Mail Date. _____ .  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____ .                                  |

## **DETAILED ACTION**

1. This Office Action is in response to the Pre-brief Appeal conference filed December 14, 2005. The finality of the rejection of the last Office action mailed May 18, 2005 is withdrawn in view of the Pre-brief Appeal conference held on December 12, 2005.

### **Status of Claims**

2. Claims 17, 19-24 are canceled. Claims 1-16, 18 and 25-28 are pending.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 8, and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Orczyk et al. (U.S. 5,937,323) in view of Redeker et al. (US 6,858,265).

Orczyk et al. teaches inserting a wafer into a reaction chamber, performing a plasma process on the wafer, cooling the wafer by an amount sufficient to terminate processing the wafer, and removing the wafer from the reaction chamber while maintaining the plasma (col. 3, lines 50-57, col. 13, lines 40-47, col. 14, lines 12-40, col. 16, lines 5-25). Orczyk et al. shows reducing the source RF power supplied to the

plasma (col. 3, lines 64-67, col. 15, lines 3-67). Orczyk et al. discloses depositing fluorine doped silicon dioxide (Abstract).

Orczyk et al. does not explicitly show creating the plasma in the reaction chamber and inserting the wafer into the reaction chamber. However, Redeker shows creating the plasma in the reaction chamber and inserting the wafer into the reaction chamber (Fig. 1-6, Abstract, col. 1, lines 10-15, col. 2, lines 25-60, col. 3, lines 25-67, col. 4, lines 1-35, col. 5, lines 17-25, col. 9, lines 25-62, col. 10, lines 1-48).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Orczyk et al. reference by including the step of creating the plasma in the reaction chamber and inserting the wafer into the reaction chamber in order to improve reliability and avoid premature release of the wafers during processing (col. 1, lines 10-15, col. 2, lines 25-60).

4. Claims 1-4, 6-11, 15-16 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwan et al. (U.S. 6,335,288) in view of Redeker et al. (US 6,858,265).

Kwan et al. teaches inserting a wafer into a reaction chamber, performing a plasma process on the wafer, cooling the wafer by an amount sufficient to terminate processing the wafer, and removing the wafer from the reaction chamber (Fig. 1D, 3, col. 13, lines 47-67, col. 14, lines 5-10, 30-40, 50-55). Kwan et al. discloses the process temperature being greater than 400°C, the second temperature being less than 250°C or less than 150°C (col. 14, lines 23-40). In addition, Kwan et al. teaches the process

being a plasma deposition of silicon dioxide for trench isolation and plasma deposition of fluorine doped silicon dioxide (Fig. 2, col. 1-10, col. 15, lines 5-25, col. 16, lines 35-36). Kwan et al. discloses a gaseous mixture is provided to the chamber and plasma is generated from this gaseous mixture to deposit some material on the substrate (col. 2, lines 57-65).

Kwan et al. does not specifically recite maintaining the plasma during removing the wafer from the reaction chamber and the specific temperature as claimed. However, Kwan et al. teaches after the second deposition is completed, the process chamber is purged by flowing an inert gas into the chamber (the plasma is maintained because the inert gas is flowing while the substrate is removed) (col. 14, lines 24-54).

Kwan et al. does not explicitly show creating the plasma in the reaction chamber and inserting the wafer into the reaction chamber. However, Redeker shows creating the plasma in the reaction chamber and inserting the wafer into the reaction chamber (Fig. 1-6, Abstract, col. 1, lines 10-15, col. 2, lines 25-60, col. 3, lines 25-67, col. 4, lines 1-35, col. 5, lines 17-25, col. 9, lines 25-62, col. 10, lines 1-48).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Kwan et al. reference by including the step of creating the plasma in the reaction chamber and inserting the wafer into the reaction chamber in order to improve reliability and avoid premature release of the wafers during processing (col. 1, lines 10-15, col. 2, lines 25-60).

Kwan et al. does not specifically show the claimed ranges. However, it would have been obvious to include the specifics ranges by routine experimentation. Where

the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

5. Claims 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwan et al. (U.S. 6,335,288) and Redeker et al. (US 6,858,265) as applied to claims 1-4, 6-11, 15-16 and 27 above, and further in view of Chang et al. (U.S. 6,143,579).

Regarding claims 14 and 18, the combination of Kwan et al. and Redeker et al. does not specifically show etching a photoresist and the wafer having a gate dielectric layer. However, Chang et al. teaches etching a photoresist and the wafer having a gate dielectric layer (col. 5, lines 28-30, 50-55).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Kwan et al. and Redeker et al. by including the steps of etching the photoresist and forming the gate dielectric layer as taught Chang et al. because Kwan et al. suggested that other variations are included within the scope of this invention (Kwan et al., col. 15, lines 13-27).

6. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwan et al. (U.S. 6,335,288) and Redeker et al. (US 6,858,265) as applied to claims 1-4, 6-11, 15-16 and 27 above, and further in view of Wang et al. (U.S. 6,268,274).

Regarding claims 12-13, the combination of Kwan et al. and Redeker et al. does not specifically show depositing a phosphorous-doped silicon dioxide layer. However,

Wang et al. shows a plasma process to deposit a phosphorous-doped silicon dioxide layer (col. 6, lines 30-40).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the combination of Kwan et al. and Redeker et al. by including phosphorous-doped silicon dioxide layer as taught Wang et al. because Kwan et al. suggested that different precursors can be used to form films of different composition (Kwan et al., col. 15, lines 15-25).

#### ***Allowable Subject Matter***

7. Claims 5 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: In the examiner's opinion, it would not have been obvious to a person of ordinary skill in the art at the time of the invention to combine the references in order to meet the step of cooling the wafer before inserting the wafer into the reaction chamber because there is not motivation or suggestion.

#### ***Response to Arguments***

8. Applicant's arguments with respect to claims 1-4, 6-16, 18 and 25-27 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Langley et al. (US 5,221,414), Ngo (US 5,736,423) and Fukuda et al. (US 6,524,955) are presented as evidence to show that creating the plasma in the chamber before inserting the wafer is conventional in the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 571-272-1837.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
MARIA F. GUERRERO  
PRIMARY EXAMINER

February 9, 2006